Reg. No. : [ ][ ][ ][ ][ ][ ][ ][ ][ ][ ][ ][ ][ ]

Question Paper Code : 50447

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2017

Sixth/Seventh/Eighth Semester

Electronics and Communication Engineering

EC 6601 : VLSI DESIGN

(Common to Biomedical Engineering/Electrical and Electronics Engineering/
Electronics and Instrumentation Engineering/Medical Electronics Engineering/
Robotics and Automation Engineering)

(Regulations 2013)

Time : Three Hours
Maximum : 100 Marks

Answer ALL questions

PART – A
(10×2=20 Marks)

1. Why nMOS transistor is selected as pull down transistor ?

2. What is the need of demarcation line ?

3. Define Elmore's constant.

4. List the types of power dissipation.

5. What is NORA CMOS ?

6. Define clock jitter.

7. How to design a high speed adder ?

8. What is latency ?

9. What is ULSI ?

10. Write the various ways of routing procedure.

<center>PART – B</center> <div style="text-align: right">**(5×16=80 Marks)**</div>

11. a) i) Explain the electrical properties of CMOS. (8)

      ii) Discuss the scaling principles and its limits. (8)

<center>(OR)</center>

   b) Write the layout design rules and draw diagram for four input NAND and NOR gate. (16)

12. a) i) Draw the CMOS logic circuit for the Boolean expression Z = [A(B + C) + DE]′ and explain. (8)

      ii) Explain the basic principle of transmission gate in CMOS design. (8)

<center>(OR)</center>

   b) i) Explain the domino logic with neat diagram. (8)

      ii) Discuss the low power design principles in detail. (8)

13. a) Discuss about the design of sequential dynamic circuits and its pipelining concept. (16)

<center>(OR)</center>

   b) Explain the timing basics and clock distribution techniques in synchronous design in detail. (16)

14. a) Draw the structure of ripple carry adder and explain its operation. How the drawback in ripple carry adder overcome by carry look ahead adder and discuss. (16)

<center>(OR)</center>

   b) Design a multiplier for 5 bit by 3 bit. Explain its operation and summarize the number of adders. Discuss it over Wallace multiplier. (16)

15. a) Explain the various types of ASIC with neat diagram. (16)

<center>(OR)</center>

   b) Draw and explain the building blocks of FPGA. (16)

———————————